Remarks

Applicant has carefully reviewed the Office action dated September 19, 2005, in which the Examiner rejected claims 1-4, 6 and 7 under 35 U.S.C. 103(a) as being unpatentable over Li et al. (US 6,309,933) in view of Yagashita et al. (US 6,607,952) and Lee et al. (US 5,583,064); rejected claim 5 under 35 U.S.C. 103(a) as being unpatentable over Li et al., Yagashita et al., and Lee et al., and further in view of Bovaird (US 4,830,975).

The Rejections Under 35 U.S.C. § 103

The rejections of claims 1-4, 6, and 7 under 35 U.S.C. 103(a) as being unpatentable over Li et al. in view of Yagashita et al. and Lee et al. have been carefully considered, but are respectfully traversed.

Claim 1 recites that the low doped drain (hereinafter "LDD") is formed in the active region before forming a region where the gate will be located (step (b) in claim 1). Then, a part of the first nitride layer and the oxide layer in the LDD region is removed and the substrate corresponding to the part is etched to form the region where the gate will be located (step (d) in claim 1). By way of forming the LDD region prior to forming the region for the gate, a control of a threshold voltage is stabilized, thereby making it easier to form an ultra shallow junction that is required to a highly integrate MOSFET devices.

However, Lee et al. only discloses that a low doped drain/source is implanted after forming a pattern for a channel region of a transistor. In Lee et al., the channel region is formed by etching Si_3N_4 layer 53 and 63 (column 5, lines 12-15, and Fig. 5B, and column 6, lines 25-28, and Fig. 6B), and then an ion implantation to form the LDD region is carried out (column 5, lines 30-34, and Fig. 5D, and column 6, lines 61-65, and Fig. 6H).

As found in the response to the prior Office action of March 8, 2005, Li et al. only discloses that the LDD implantation may be formed by an angled LDD ion implantation after the gate is formed (column 5, lines 56-57). Further, Li et al. does not disclose selectively forming a shallow trench isolation in a substrate.

As also found in the response to the prior Office action, Yagashita et al. discloses a method of manufacturing a semiconductor device which has a trench formed in an element

isolation region surface of the substrate. However, Yagashita et al. does not disclose that a part of the LDD formed in the active region is removed for forming the region for the gate.

Accordingly, although Yagashita et al. discloses the shallow trench isolation, combination of Li et al., Yagashita et al., and Lee et al. cannot render the pending claims obvious because none of Li et al., Yagashita et al., and Lee et al. disclose or even imply implanting the LDD prior to forming the region where the gate will be located. By way of performing the ion implantation to form the LDD region before forming the region where the gate will be located, the control of the threshold voltage is stabilized to make it easier to form the ultra shallow junction, and a step of ion implantation is more easily performed so that the effectiveness of the entire process for manufacturing the MOSFET devices can be improved. Accordingly, the difference in the order in which the steps of the claims are conducted results in an unexpected effect and can be patentable.

Accordingly, even if every single disclosure contained in each of the references is selectively chosen and stacked together against the claims, such a combination cannot possibly suggest to a person having ordinary skill in the art the inventive features recited.

It is also believed that claims 2-4, 6, and 7 directly depending on claim 1 are allowable for the same reasons indicated with respect to the claim 1, and further because of the additional features recited therein which, when taken alone and/or in combination with the features recited in the claim 1, remove the claims even further from the disclosures made in the cited references.

The Examiner stated that Bovaird discloses thin oxide layer formed by a wet oxidation method at a temperature of 750°C, and therefore, claim 5 is obvious over the combination of Li et al., Yagashita et al., Lee et al., and Boviard. However, Bovaird does not disclose the method for forming the LDD. Accordingly, the combination of Li et al., Yagashita et al., Lee et al., and Boviard does not teach that a part of the LDD formed in the active region is removed for forming the region for the gate. Accordingly, it is respectfully submitted that claim 5 defines an unobvious and patentable invention over and above the reference and is, therefore, allowable.

CONCLUSION

Applicant believes that this is a full and complete response to the Office action. For the reasons discussed above, Applicant now respectfully submits that all of the pending claims are in complete condition for allowance. Accordingly, it is respectfully requested that the Examiner's rejections be withdrawn; and that claims 1-7 be allowed in their present forms. If the Examiner feels that any issues that remain require discussion, he is kindly invited to contact applicant's undersigned attorney to resolve the issues.

Should the Examiner require or consider it advisable that the specification, claims an/or drawings be further amended or corrected in formal respects, in order to place the case in condition for final allowance, then it is respectfully requested that such amendment or correction be carried out by Examiner's Amendment and the case be passed to issue.

Alternatively, should the Examiner feel that a personal discussion might be helpful in advancing this case to allowance, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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